[Claim 39] 39. An integrated circuit, comprising:

a copper damascene or dual damascene wire in a fluorinated silicon glass dielectric layer, a top surface of said copper damascene or dual damascene wire coplanar with a top surface of said fluorinated silicon glass dielectric layer;

a first capping layer formed on said top surface of said copper damascene or dual damascene wire and said top surface of said fluorinated silicon glass dielectric layer; and

a second capping layer formed on said top surface of said first capping layer, said first capping layer thin enough to allow performance of one or more characterization procedures in relation to said integrated circuit and thick enough to prevent formation, on said top surface of said copper damascene or dual damascene wire, of copper containing particles by reaction of copper in said copper damascene or dual damascene wire with fluorine in said fluorinated silicon glass dielectric layer.

[Claim 40] 40. The structure of claim 38, wherein said fluorinated silicon glass dielectric layer comprises about 1% to about 9% by weight of fluorine.

[Claim 41] 41. The structure of claim 38, wherein said first capping layer and said second capping layer independently

include a material selected from the group consisting of Si_xN_y, Si_xC_y, SiC_xH_y, $SiC_xO_yN_z$ and SiC_xN_y.

[Claim 42] 42. The structure of claim 38, wherein said first capping layer and said second capping layer independently include one or more layer of materials selected from the group consisting of Si_xN_y, Si_xC_y, SiC_xH_y, $SiC_xO_yN_z$ and SiC_xN_y.

[Claim 43] 43. The structure of claim 38, wherein said first capping layer has a thickness between about 100 Å and 300 Å.

[Claim 44] 44. The method of claim 38, wherein said second capping layer has a thickness between about 150 Å and 700 Å.

[Claim 45] 45. The method of claim 38, wherein said second capping layer is a copper diffusion barrier.

[Claim 46] 46. The method of claim 38, wherein said first capping layer in combination with said second capping layer is a copper diffusion barrier.

[Claim 47] 47. The method of claim 38, wherein said one or more characterization procedures are selected from the group

consisting of optical or SEM inspection, optical or SEM image size measurement and electrical probing.

[Claim 48] 48. The method of claim 38, wherein said first capping layer is thin enough to be transparent to visible light, to back-scattered electrons in a SEM or to both.

[Claim 49] 49. The method of claim 38, wherein said first capping layer is thin enough to allow penetration of said first capping layer by a point of a conductive probe tip in order to make electrical contact to said copper damascene or dual damascene wire.

[Claim 50] 50. A method of manufacturing an interconnect, comprising:

(a) providing a substrate;

(b) forming a copper wire in a dielectric layer, said dielectric layer having a top surface;

(c) exposing a copper top surface of said copper wire, said copper top surface of said copper wire coplanar with said top surface of said dielectric layer or exposing said copper top surface of said copper wire in a bottom of a trench formed in said dielectric layer;

after step (c), (d) storing said substrate in a controlled environment; and

after step (d), (e) performing further processing steps on said substrate.

[Claim 51] 51. The method of claim 49, wherein said dielectric layer comprises fluorinated silicon glass.

[Claim 52] 52. The method of claim 49, wherein said controlled environment is selected from the group consisting of humidity controlled environment, temperature controlled environments, inert gas environments, non-oxygen containing environments and combinations thereof.

[Claim 53] 53. The method of claim 49, wherein said controlled environment has a relative humidity of about 20% or less at a temperature of about 70°F or less.

[Claim 54] 54. The method of claim 49, wherein said controlled environment comprises H_2, He, Ar, N_2, combinations H_2, He, Ar, N_2, or air with a relative humidity of about 20% or less.

[Claim 55] 55. A method of manufacturing an interconnect, comprising:

(a) providing a substrate;

(b) forming a copper wire in a dielectric layer, said dielectric layer having a top surface;

(c) exposing a copper top surface of said copper wire, said copper top surface of said copper wire coplanar with said top surface of said dielectric layer or exposing said copper top surface of said copper wire in a bottom of a trench formed in said dielectric layer to an ambient atmosphere for a period of time;

after step (c), (d) if said period of time exceeds a predetermined period of time, performing a rework clean or a rework chemical mechanical polish; and

after step (d), (e) performing further processing steps on said substrate.

[Claim 56] 56. The method of claim 54, wherein said dielectric layer comprises fluorinated silicon glass.

[Claim 57] 57. The method of claim 54, wherein step (e) includes forming a capping layer over said dielectric layer.

[Claim 58] 58. The method of claim 54, wherein said rework clean includes etching in an aqueous solution containing HF.

[Claim 59] 59. The method of claim 54,

wherein formation of said copper wire includes a first chemical mechanical polish of a copper layer formed over a non-copper liner layer followed by a second chemical mechanical polish of said liner layer; and

wherein said rework chemical mechanical polish is the same process as said second chemical mechanical polish for about the same or less time.

[Claim 60] 60. The method of claim 54, further including:

after step (e), (f) determining an elapsed time from formation of said capping layer to a present time;

after step (f), (g) if said elapsed time exceeds a additional predetermined period of time, performing a cryogenic clean; and

after step (g), (h) forming an additional capping layer on a top surface of said capping layer.